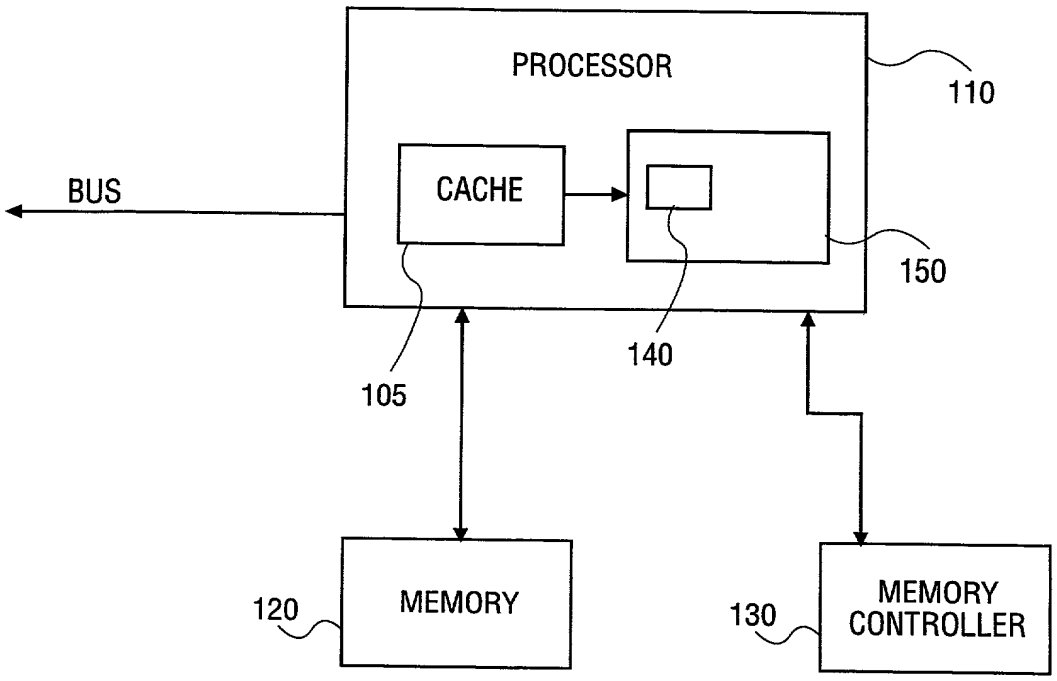
PROCESSOR
110
BUS
CACHE
150
105
140
120
MEMORY
130
MEMORY CONTROLLER

FIG. 1

0062ET 962.2S/60

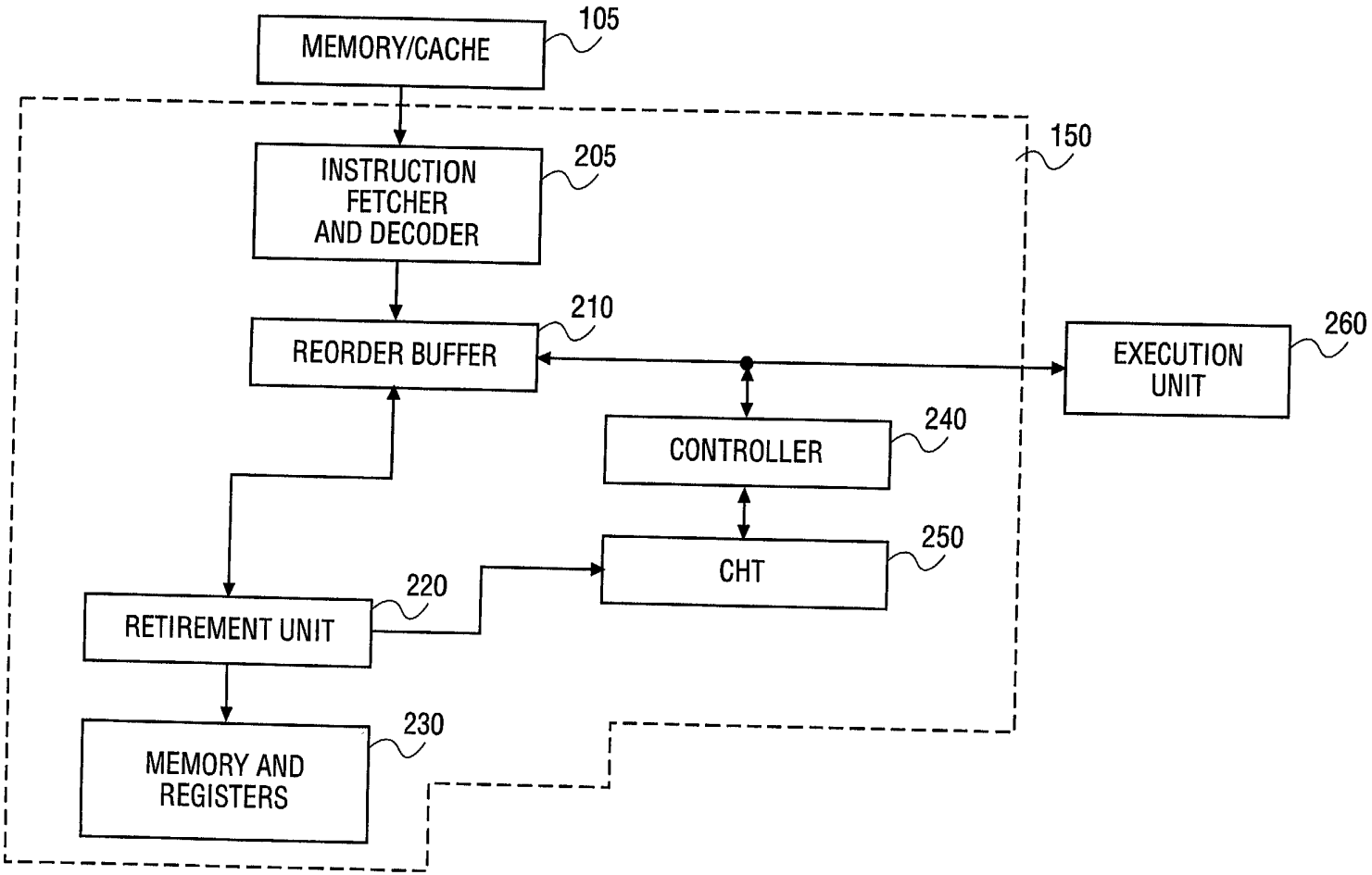

FIG. 2

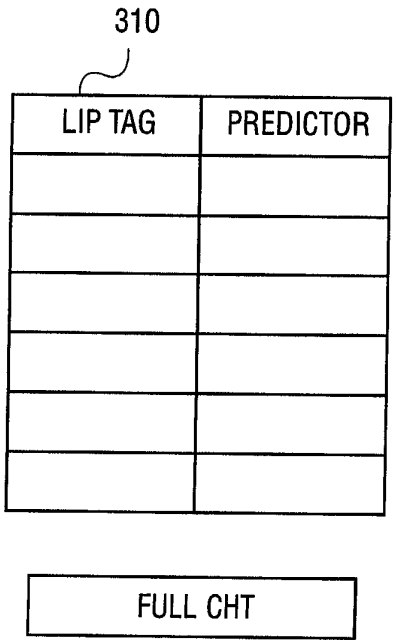

FIG. 3

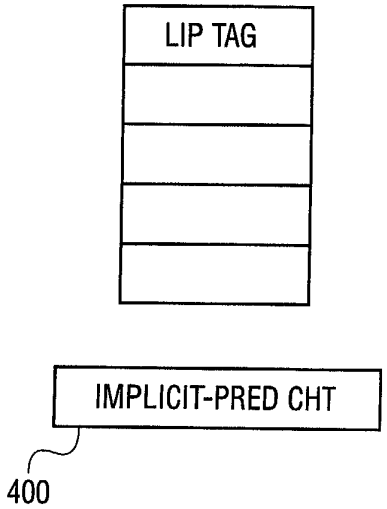

FIG. 4

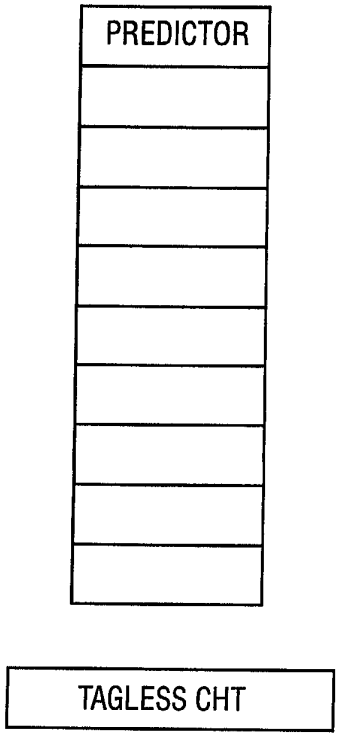

FIG. 5

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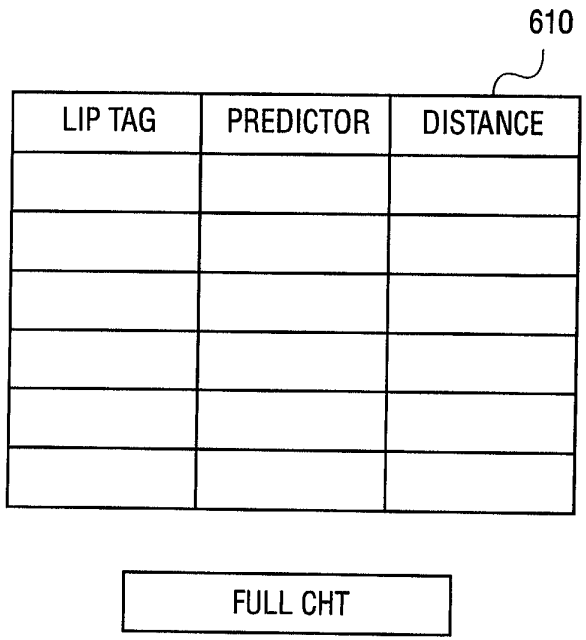


FIG. 6

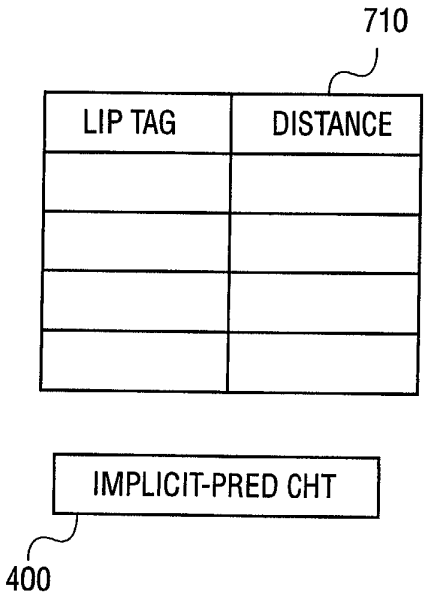


FIG. 7

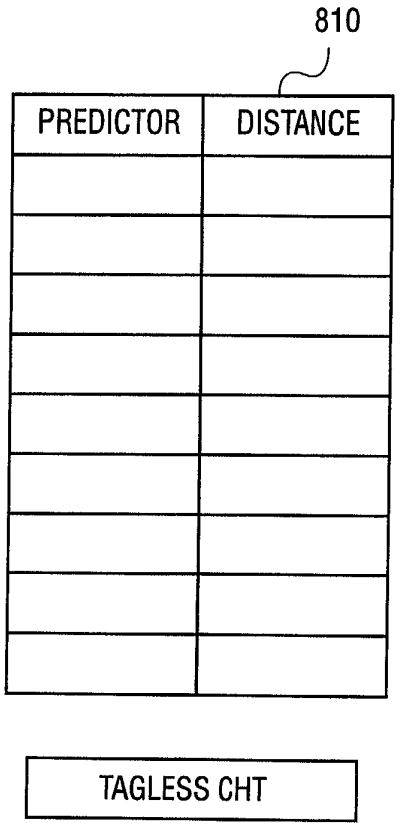
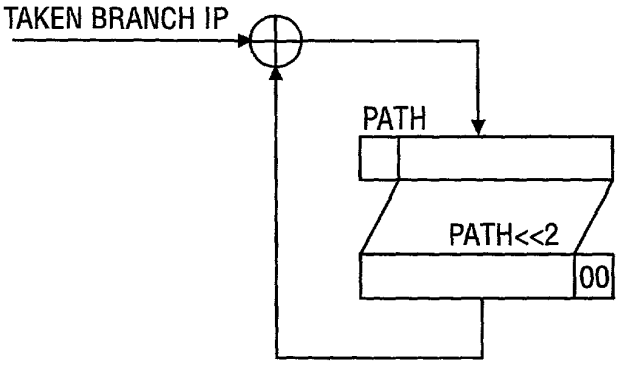
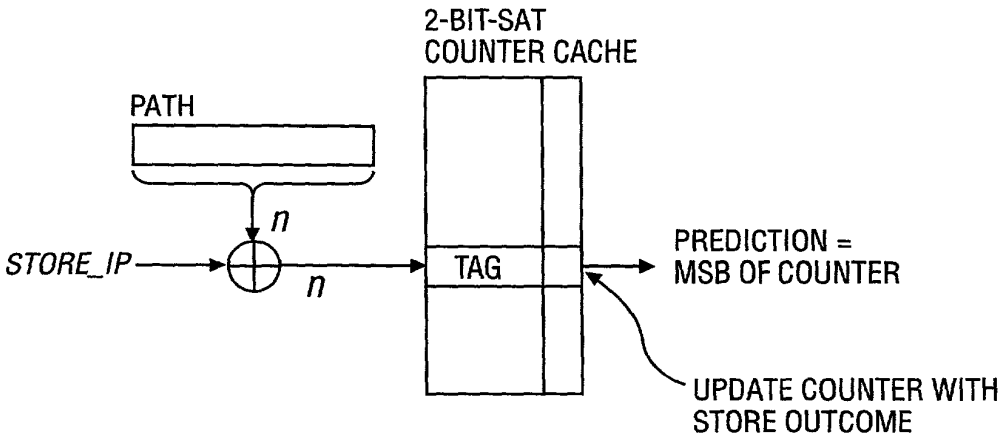


FIG. 8



PATH UPDATE. NEW_PATH = (OLD_PATH<<2) XOR TAKEN_BRANCH_IP

FIG. 9



PREDICTOR INDEXING: INDEX = STORE_IP XOR PATH

FIG. 10

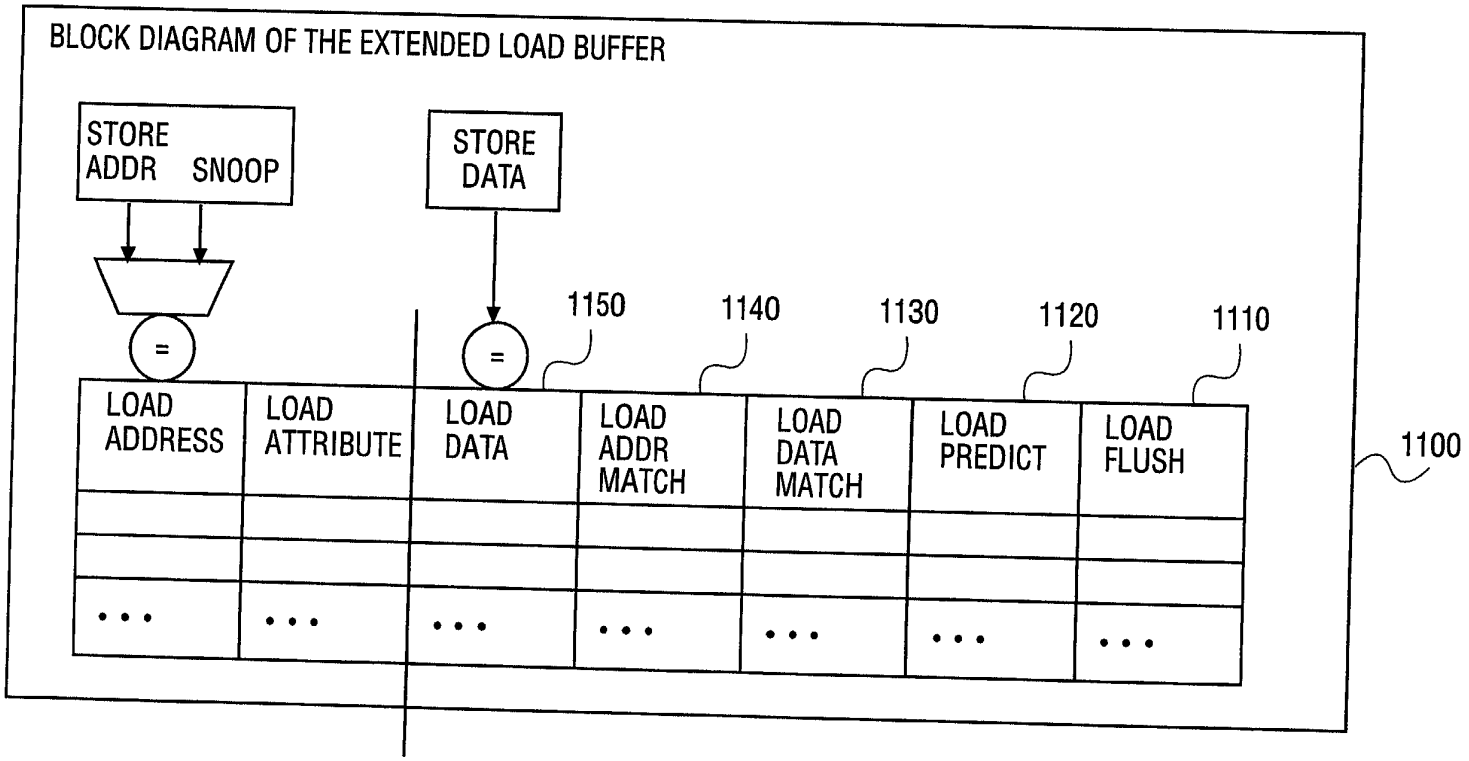

BLOCK DIAGRAM OF THE EXTENDED LOAD BUFFER
STORE ADDR SNOOP
STORE DATA
=
=
1150
1140
1130
1120
1110
LOAD ADDRESS
LOAD ATTRIBUTE
LOAD DATA
LOAD ADDR MATCH
LOAD DATA MATCH
LOAD PREDICT
LOAD FLUSH
1100

FIG. 11

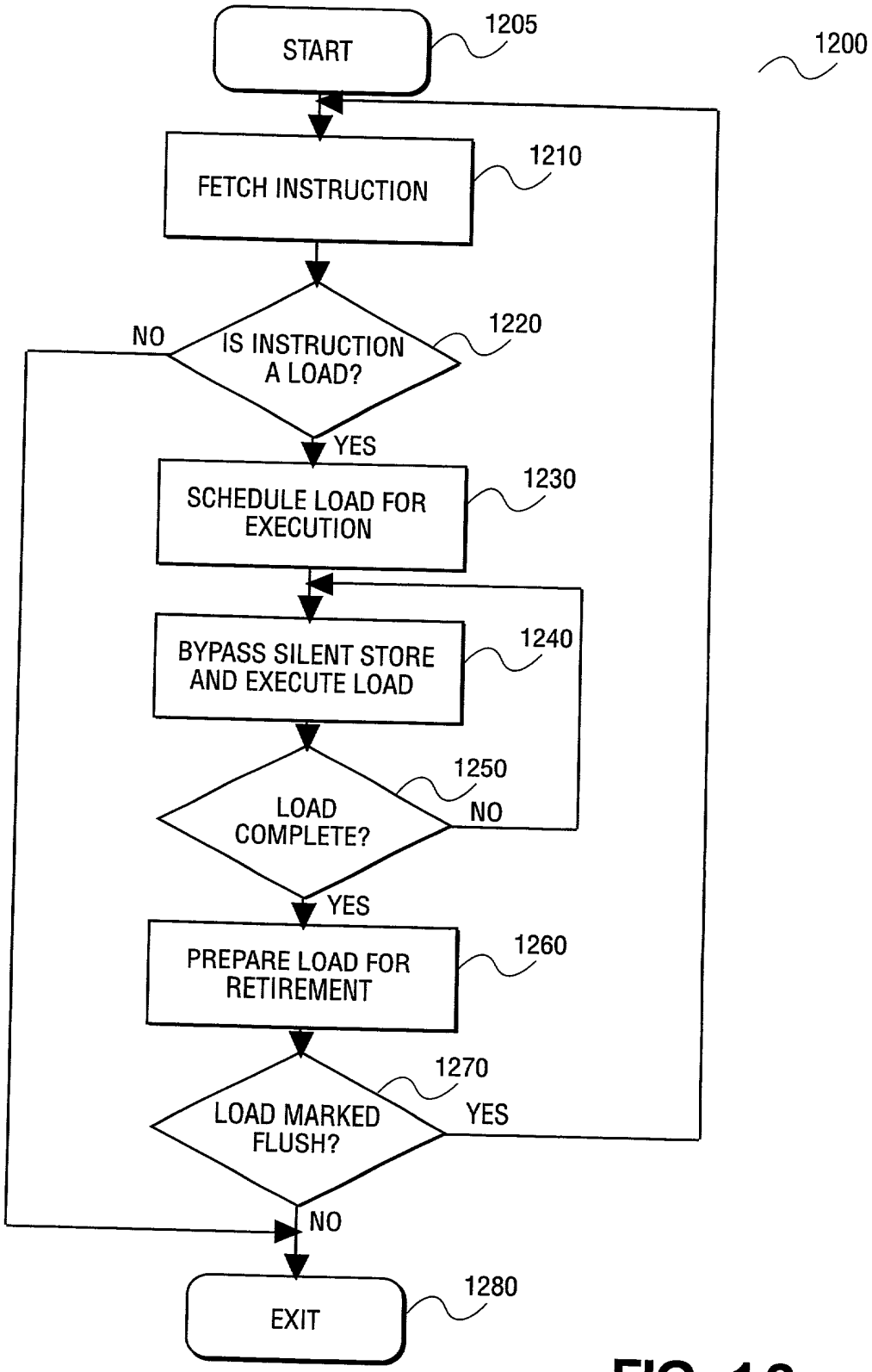

START
1205
1200
FETCH INSTRUCTION
1210
IS INSTRUCTION A LOAD?
1220
NO
YES
SCHEDULE LOAD FOR EXECUTION
1230
BYPASS SILENT STORE AND EXECUTE LOAD
1240
LOAD COMPLETE?
1250
NO
YES
PREPARE LOAD FOR RETIREMENT
1260
LOAD MARKED FLUSH?
1270
YES
NO
EXIT
1280

FIG. 12

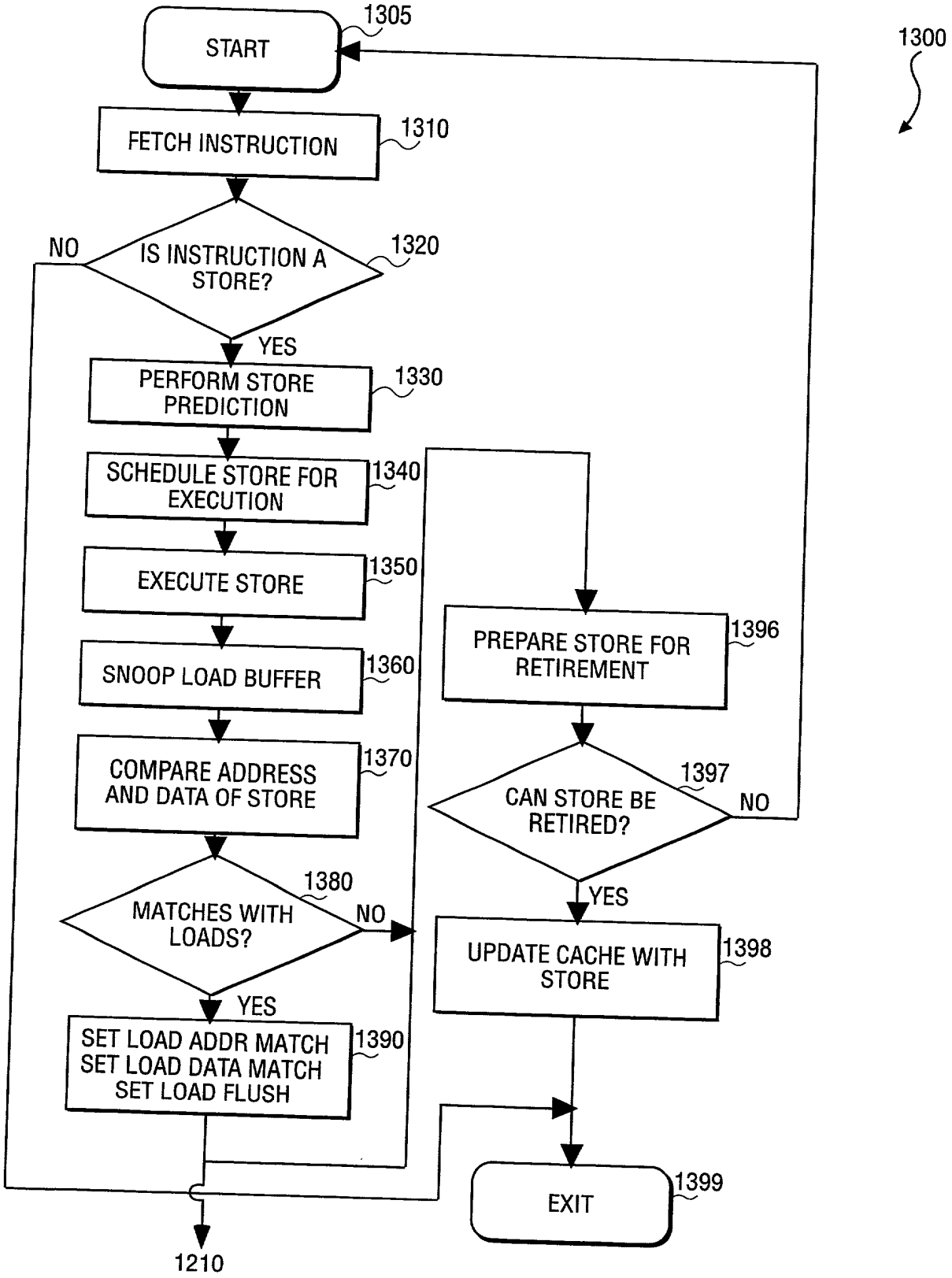

1300
START
1305
FETCH INSTRUCTION
1310
IS INSTRUCTION A STORE?
1320
NO
YES
PERFORM STORE PREDICTION
1330
SCHEDULE STORE FOR EXECUTION
1340
EXECUTE STORE
1350
SNOOP LOAD BUFFER
1360
COMPARE ADDRESS AND DATA OF STORE
1370
MATCHES WITH LOADS?
1380
NO
YES
SET LOAD ADDR MATCH
SET LOAD DATA MATCH
SET LOAD FLUSH
1390
1210
PREPARE STORE FOR RETIREMENT
1396
CAN STORE BE RETIRED?
1397
NO
YES
UPDATE CACHE WITH STORE
1398
EXIT
1399

FIG. 13